# INDIAN INSTITUTE OF TECHNOLOGY GUWAHATI



# EE 311: VLSI LAB

July-Nov 2016

Assignment 4

6th September 2016

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**NOTE: IF PICTURE ARE UNCLEAR, SCREENSHOTS ARE THERE IN FOLDER.**

# Objective:

To design an AND Gate using NAND Gate and NOT Gate with following specification:

1. Input Frequency, f = 400 MHz

2. Load Capacitance, CL = 300 fF

3. Worst case risetime, falltime = 5 % of input time period

**Calculations:**

Given input frequencies = 400 MHz. Therefore time period of input T = 2.5ns.

Rise Time, tr = Fall Time, tf = 5 % of T

=> tr = tf = 0.05 \* 2.5 ns = 0.125ns

This is the worst case scenario. We have to keep the risetime and falltime less than this.

We can find charging and discharging of capacitor between 10% to 90% using following equation:

t = 2.2 \* Req \* CL

Since,

t <= tr

=> 2.2 \* Req \* CL <= 0.125ns

=> Req <= 189.4 Ω ------------------------------------(i)

For NMOS,

RNORM = 3660 Ω, and since Req = RNORM / mn where mn is the multiplicity of NMOS,

=> mn >= 19.32

For PMOS,

RNORM = 10980 Ω, and since Req = RNORM / mp where mp is the multiplicity of PMOS,

=> mp >= 58

So for this assigment, I have chosen mn = 24 and mp = 60.

Therefore expected value of risetime:

t = 2.2 \* Req \* CL

=> tr = 120.78 ps

Therefore expected value of falltime:

t = 2.2 \* Req \* CL

=> tr = 100.65 ps

Hence width chosen was for PMOS, with finger = 2:

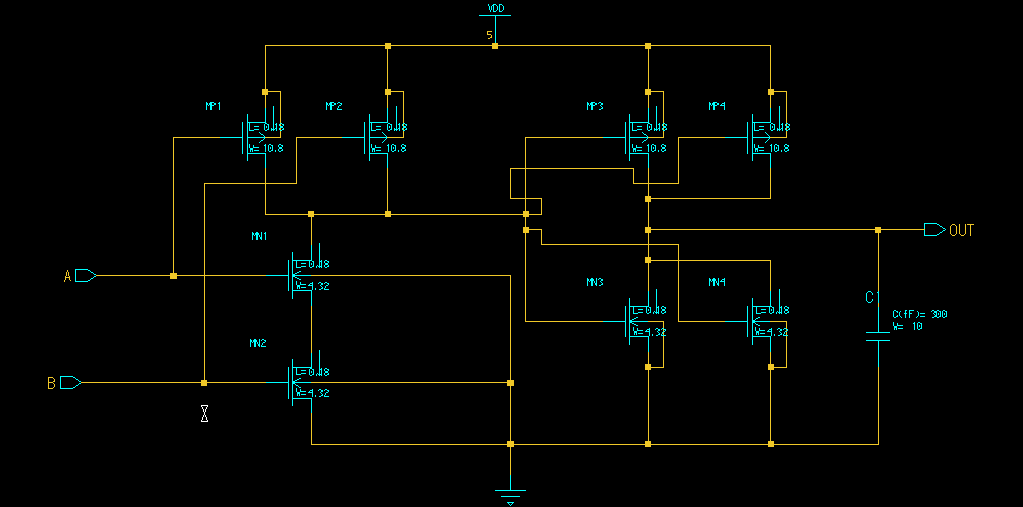
w = (mp / 2) \* 0.36 = 10.8u

Hence width chosen was for NMOS, with finger = 2:

w = (mn / 2) \* 0.36 = 4.32u

**Schematic:**

**1. Screenshot:**



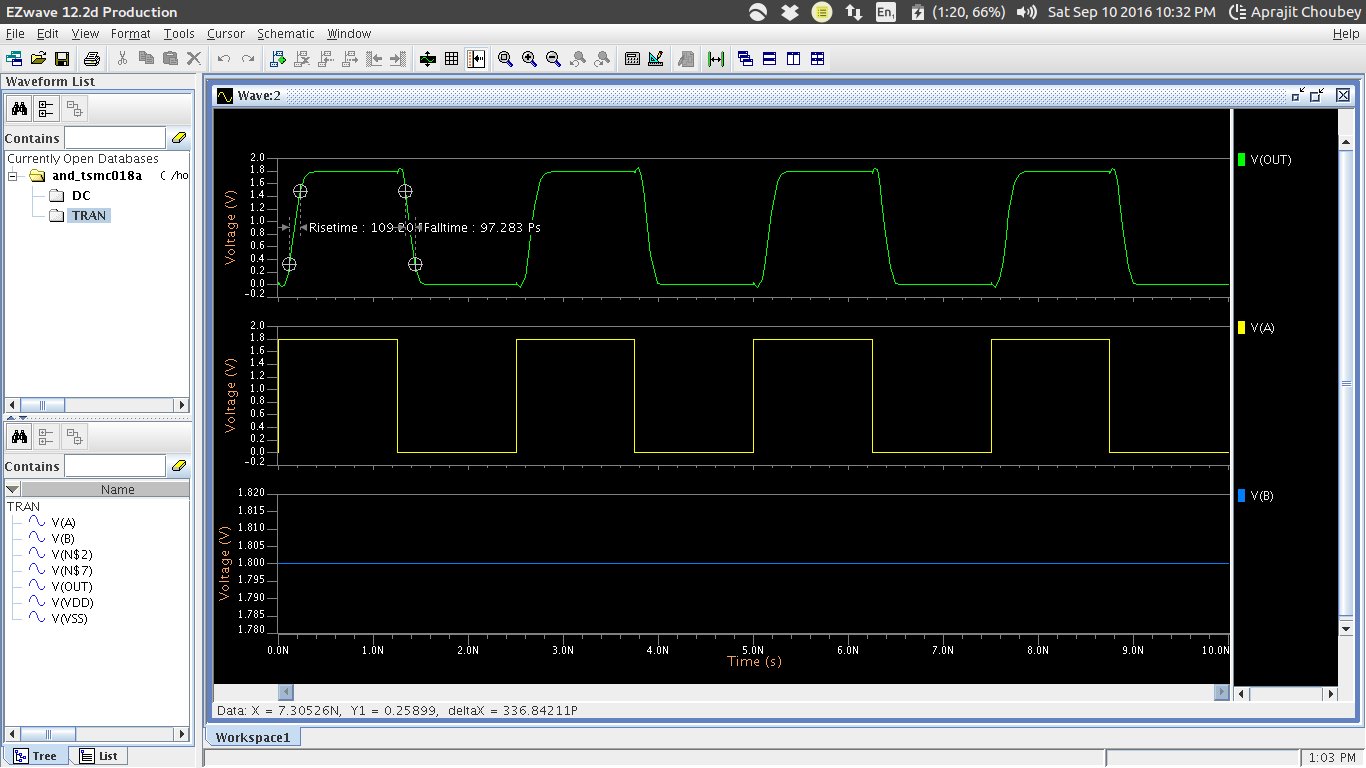
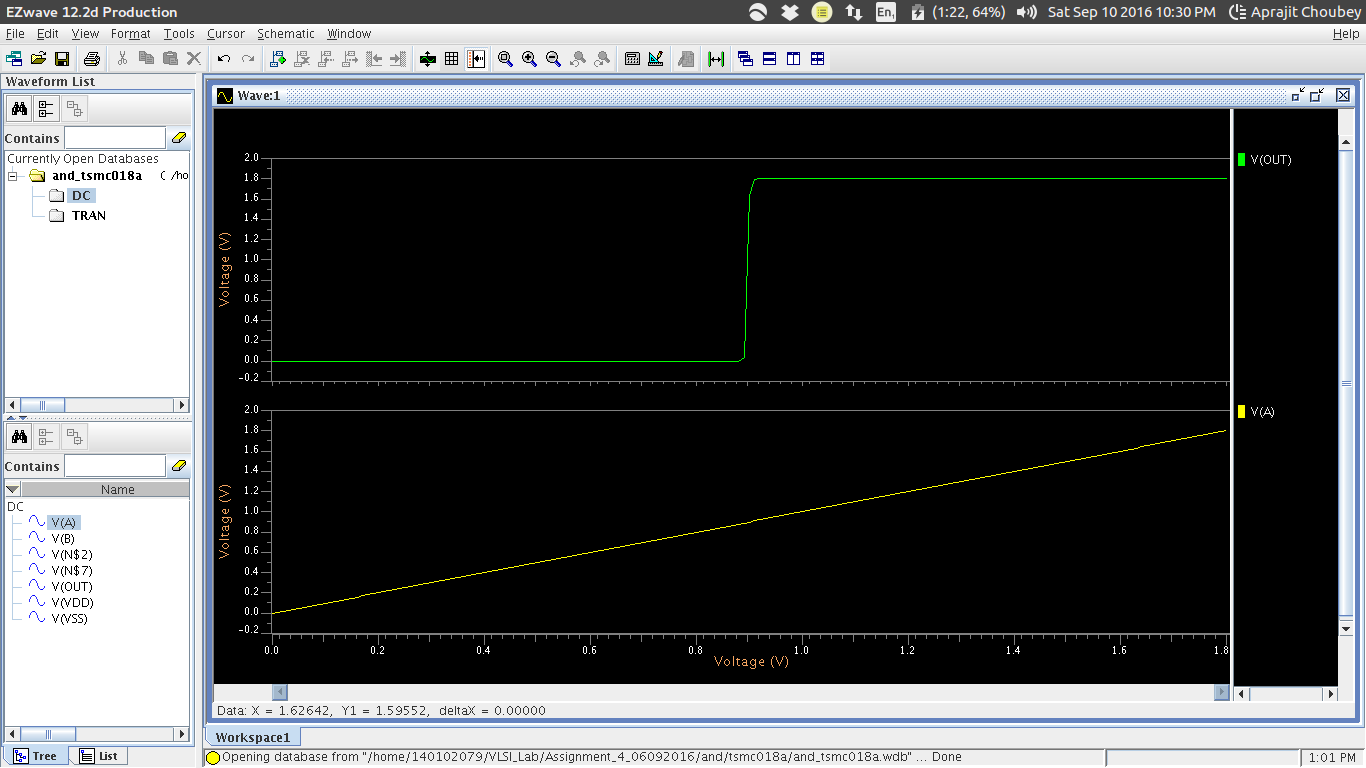
**Observed:**

1. Case I: Rise Time = 109.204ps Fall Time = 97.283ps

2. Case II: Rise Time = 114.09ps Fall Time = 101.59ps

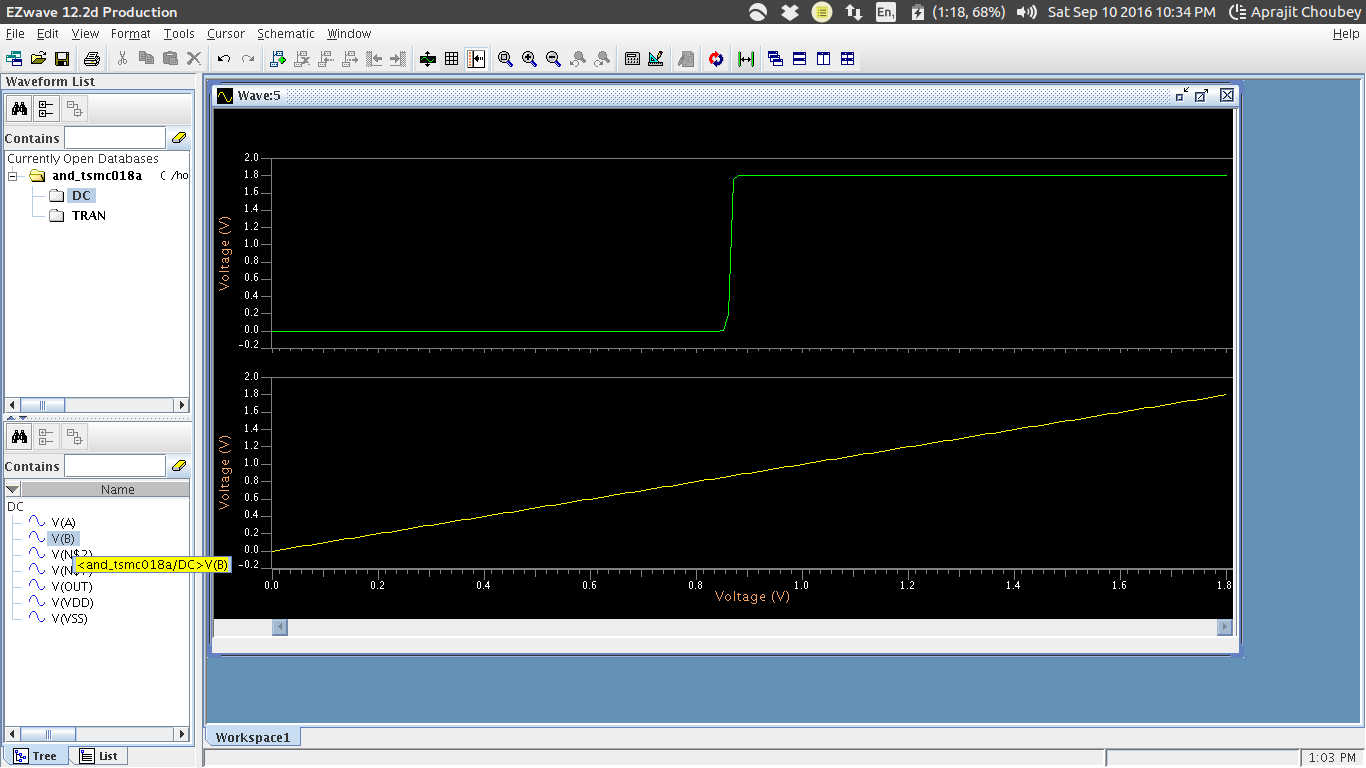
**2. Simulation:**

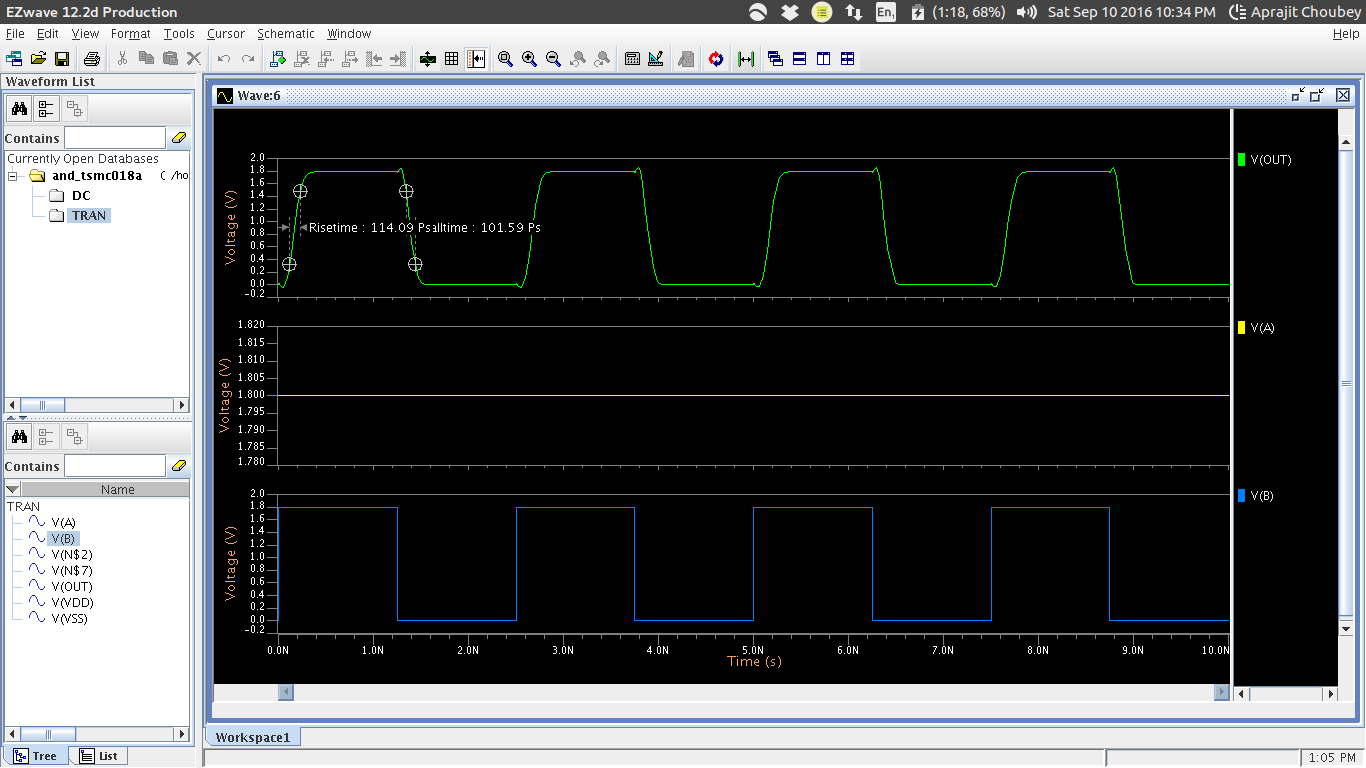
**I) A – Pulse, B – High**



**2. Simulation:**

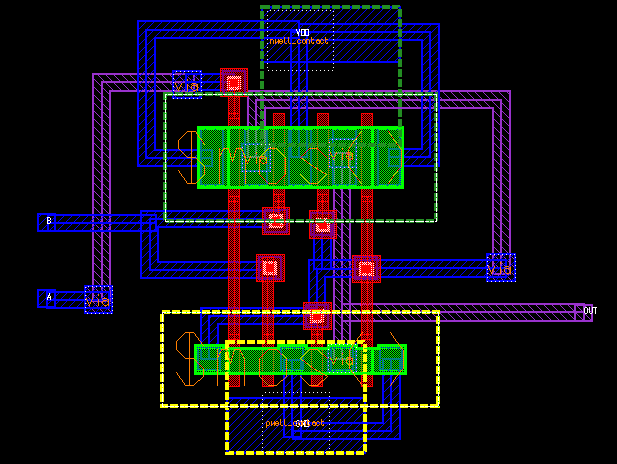
**I) A – Pulse, B – High**





**Layout:**

**1. Screenshot:**



**Observed:**

1. Rise Time = 118.85ps Fall Time = 113.33ps

**2. Post Layout Simulation:**

